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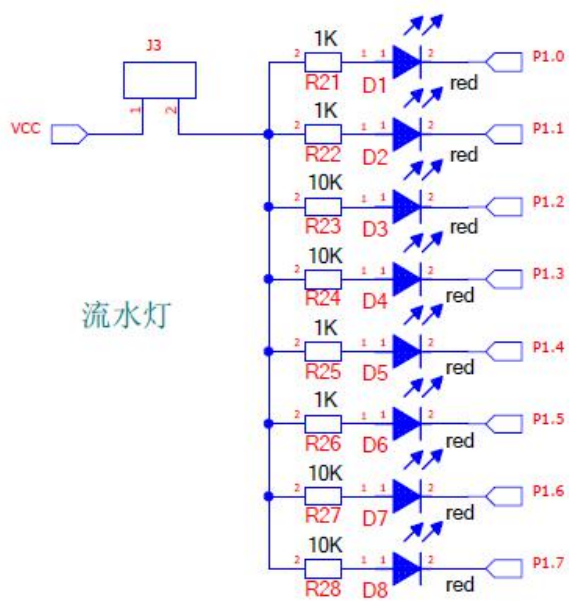
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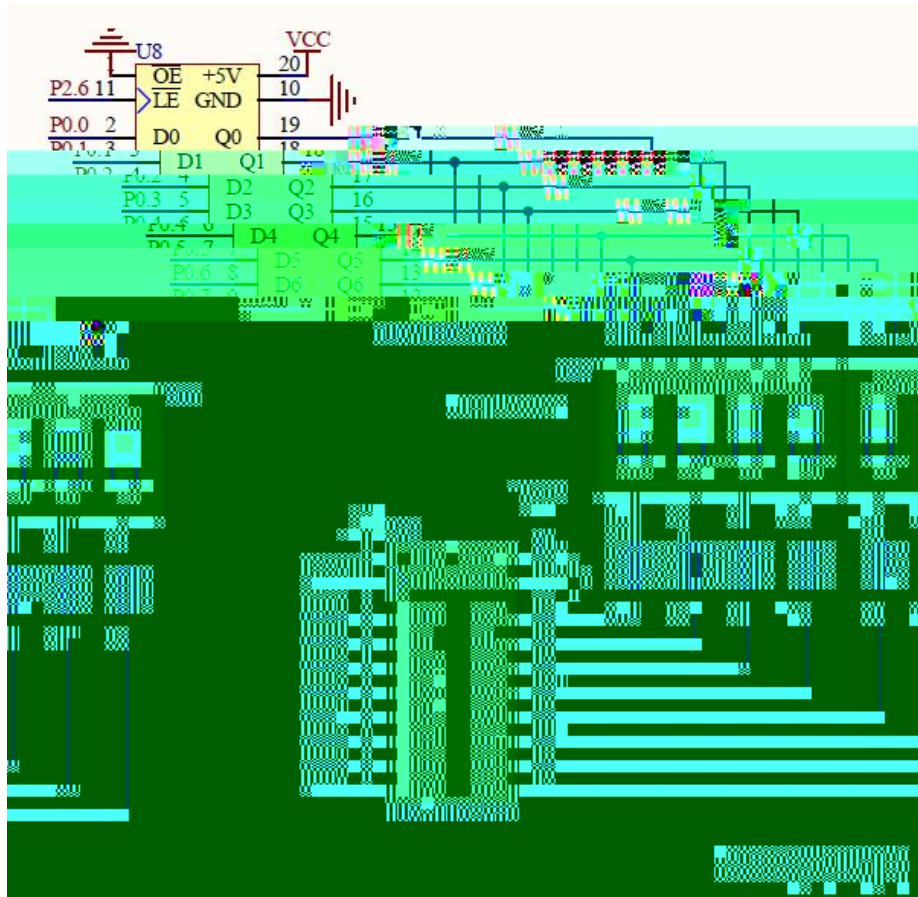
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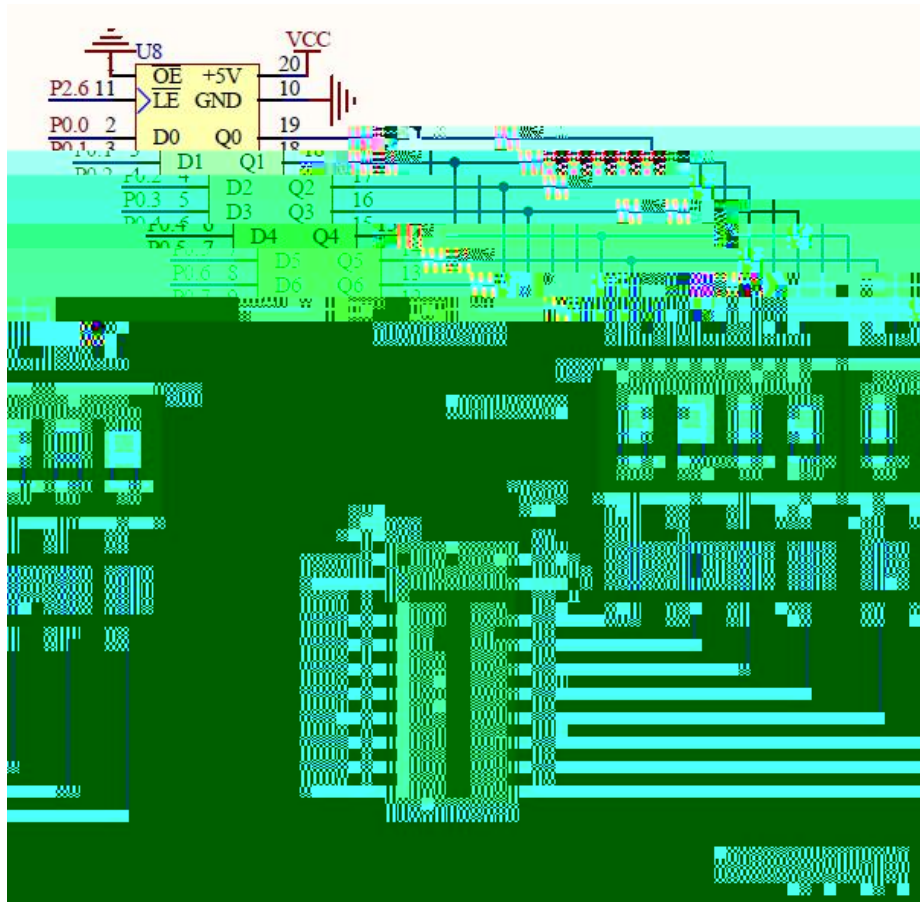


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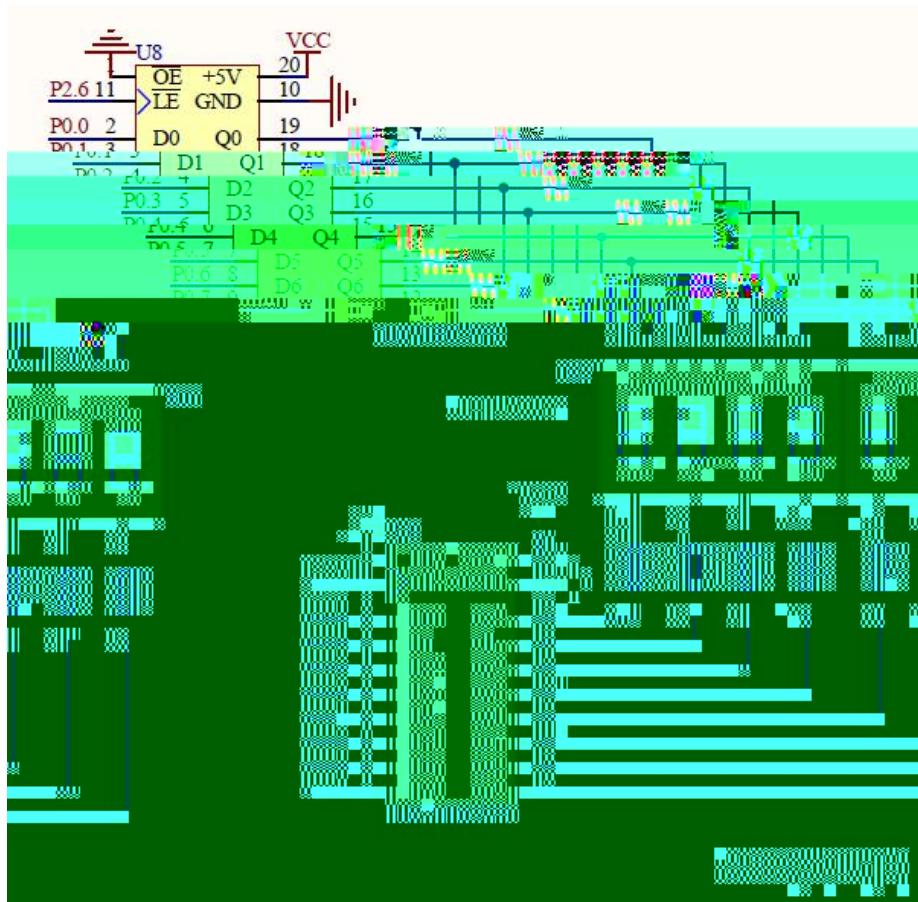
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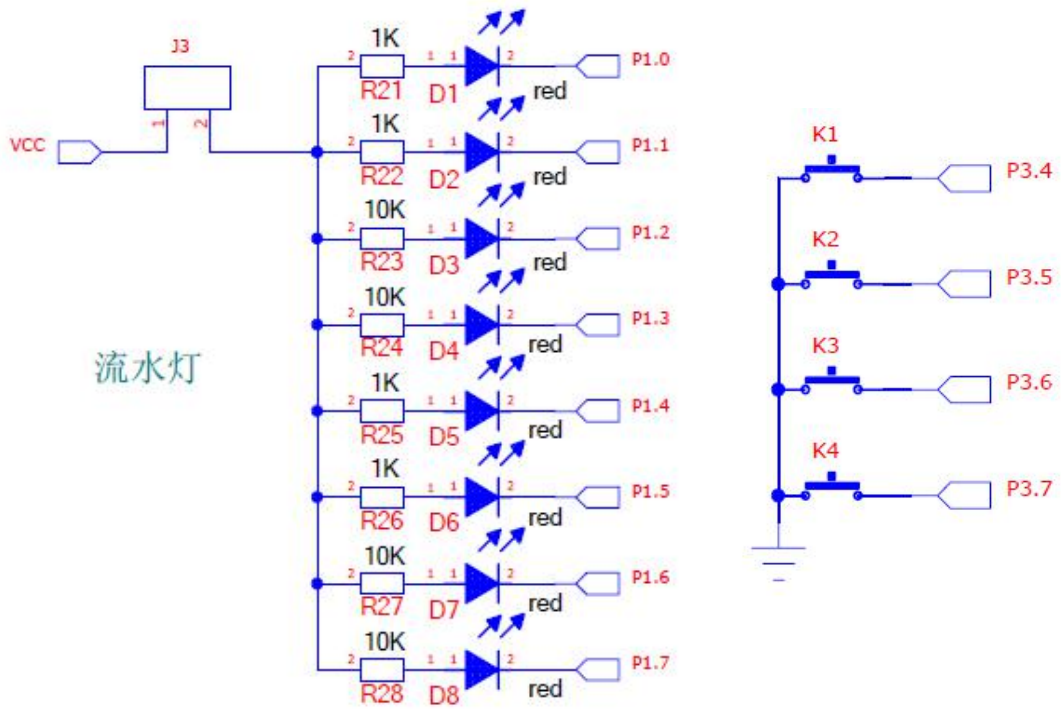
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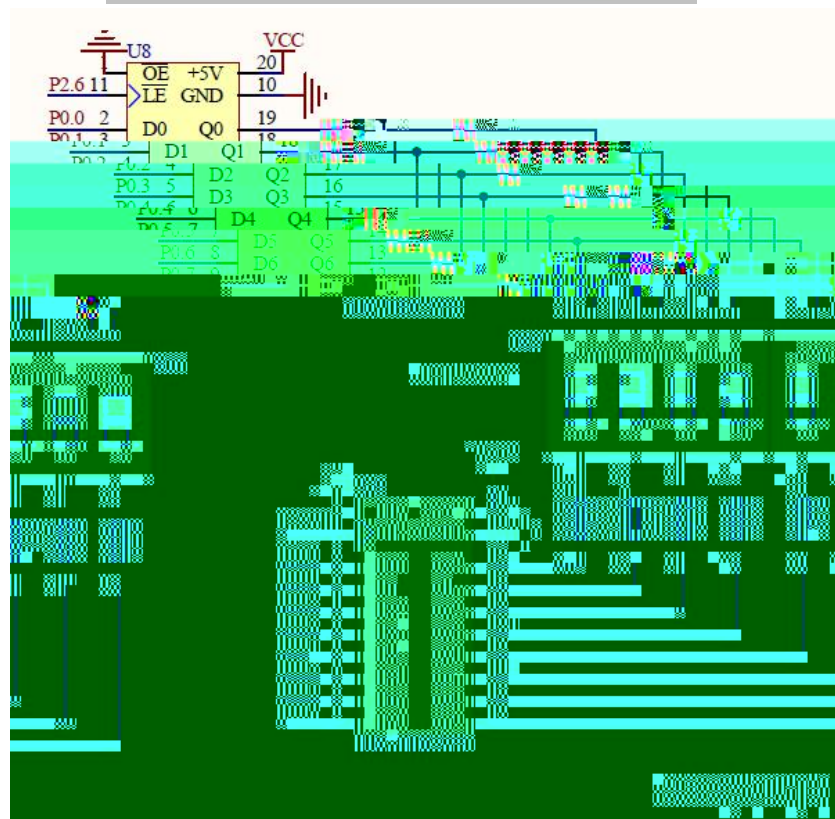
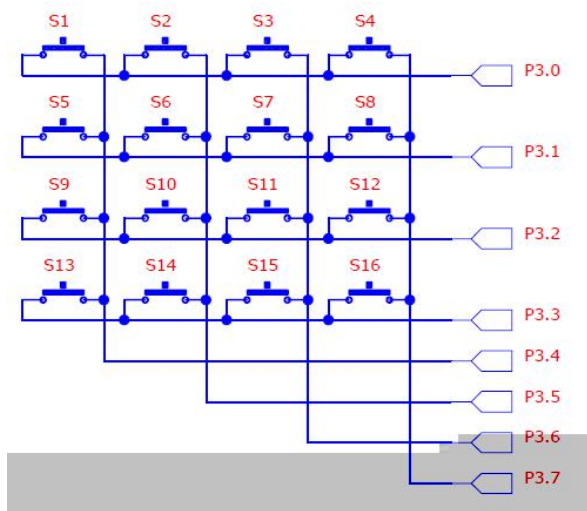
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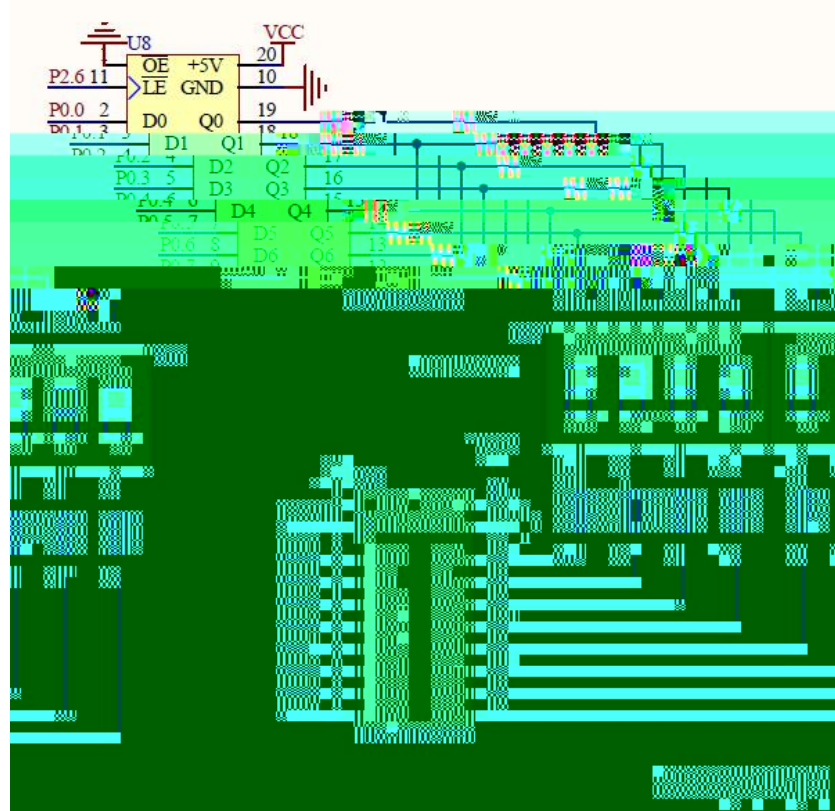
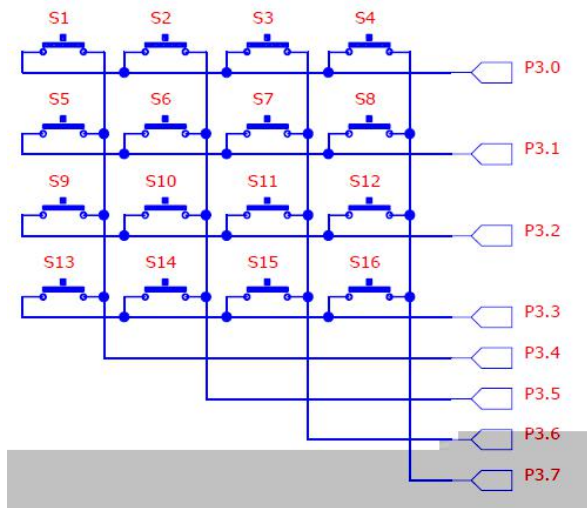
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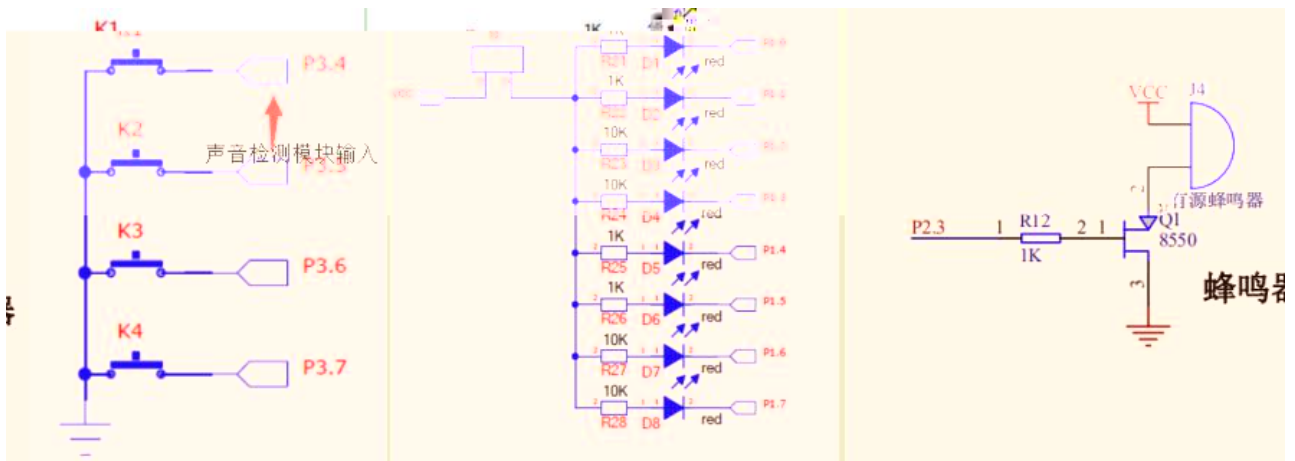
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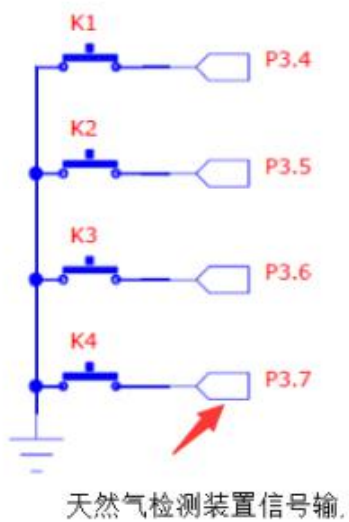
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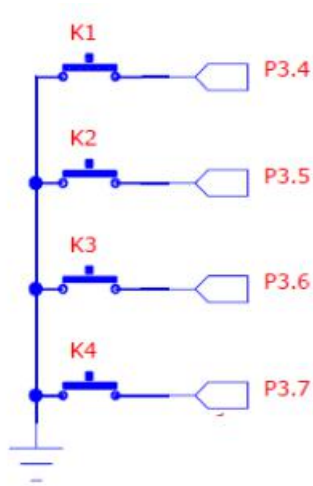
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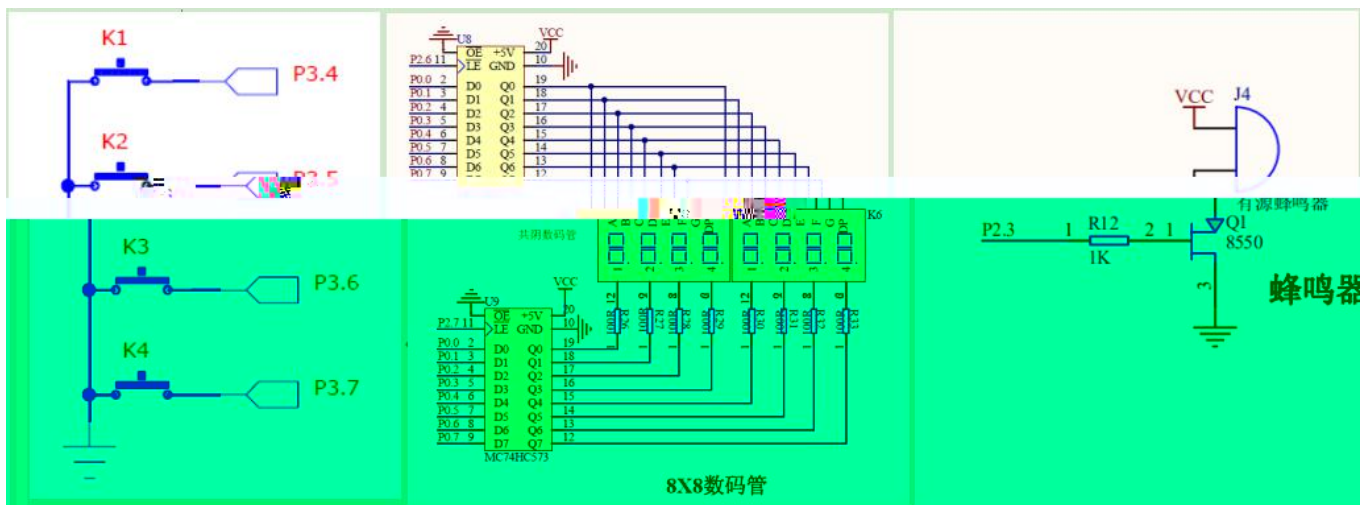
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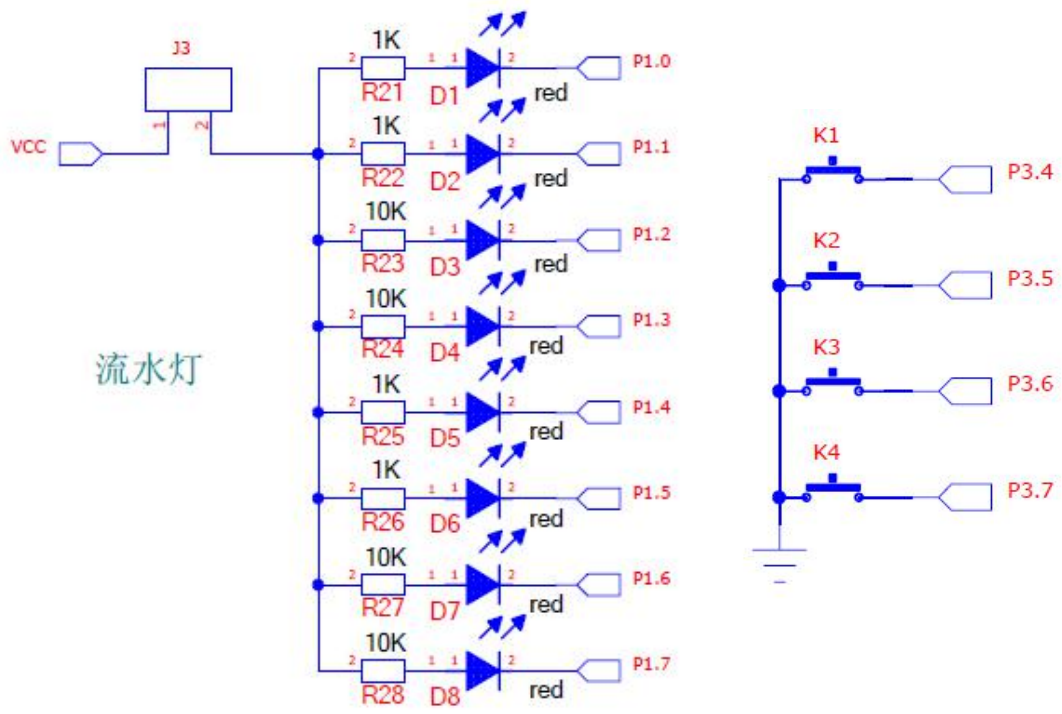
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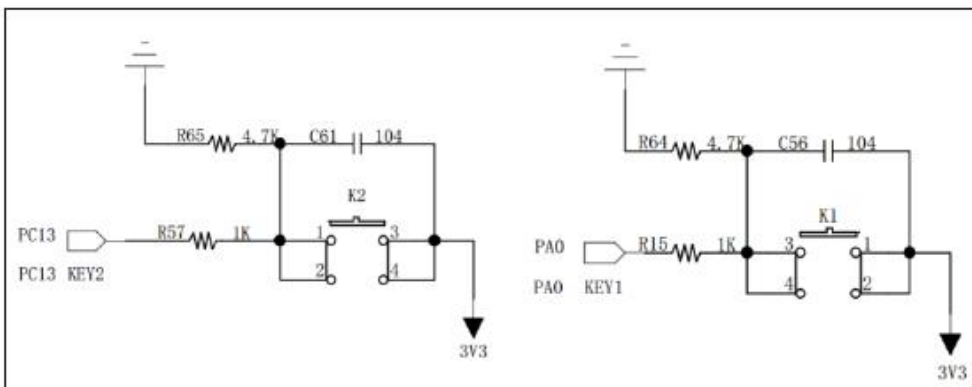
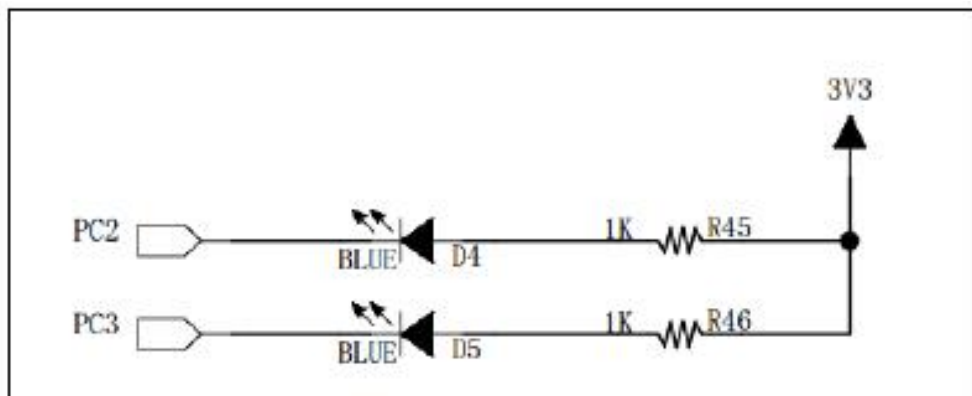
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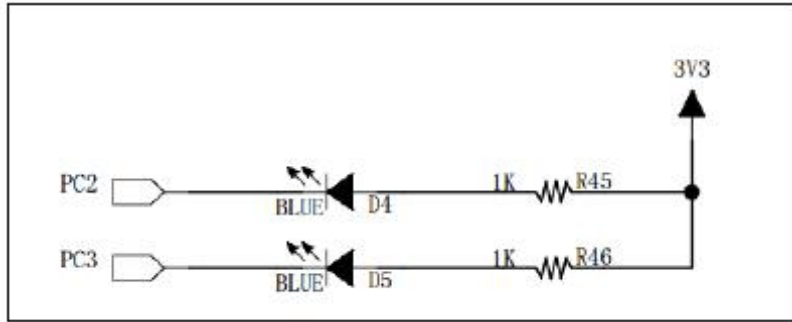
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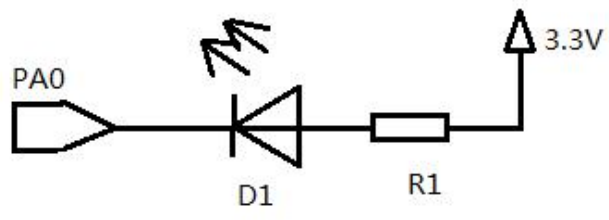
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2	PC13/ANT1	VSS	63
3	PC14/OSC32	PB9/TIM4_CH4/SDIO_D5	62
4	PC15/OSC32	PB8/TIM4_CH3/SDIO_D4	61
5	PD0/OSCIN	PA7/I2C1_SCL/TIM4_CH2	60
6	PD1/OSCOUT	PA6/I2C1_SDA/TIM4_CH1	59
7	NRES	PB5/I2C1_SMBA/SPI3_MOSI/I2S3_SD	58
8	PC0/ADC10	PB4/JNTRST/SPI3_MISO	57
9	PC1/ADC11	PB3/JTDO/SPI3_SCK/I2S3_CK	56
10	PC2/ADC12	PC2/U5_RX/TIM3_ETR/SDIO_CMD	55
11	PC3/ADC13	PC12/U5_TX/SDIO_CK	54
12	VSSA	PC11/U4_RX/SDIO_D3	53
13	VDDA	PC10/U4_TX/SDIO_D2	52
14	PA0/WKUP/ADC0/TIM2_CH1_ETR/TIM5_CH1/TIM8_ETR	PA15/JTDI/SPI3_NSS/I2S3_WS	51
15	PA1/ADC1/TIM2_CH2/TIM5_CH2	PA14/JTCK/SWCLK	50
16	PA2/U2_TX/ADC2/TIM2_CH3/TIM5_CH3	VDD	49
17	PA3/U2_RX/ADC3/TIM2_CH4/TIM5_CH4		48
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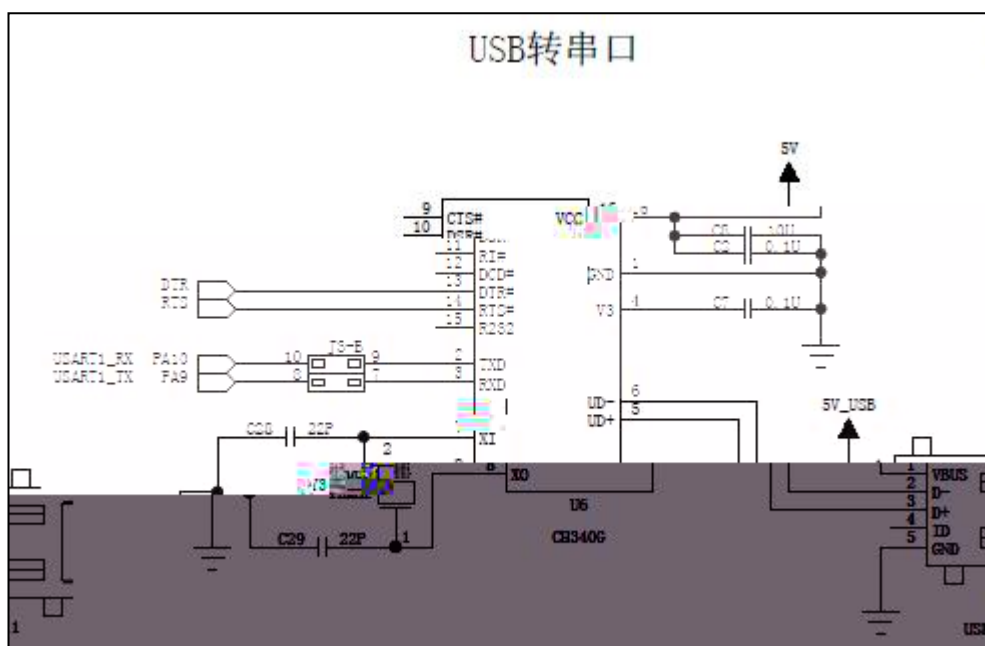
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2	PC13/ANT1	VSS	63
3	PC14/OSC32	PB9/TIM4_CH4/SDIO_D5	62
4	PC15/OSC32	PB8/TIM4_CH3/SDIO_D4	61
5	PD0/OSCIN	DD07/I2C1_SDA/L1A/TIM4_CH2	59
6	PD1/OSCOUT	PB6/I2C1_SCL/TIM4_CH1	58
7	NRS*	PB5/I2C1_SMBA/SPI3_MOSI/I2S3_SD	57
8	PC0/ADC10	PB4/JNTRST/SPI3_MISO	56
9	PC1/ADC11	PB3/JTDO/SPI3_SCK/I2S3_CK	55
10	PC2/ADC12	PC2/U5_RX/TIM3_ETR/SDIO_CMD	54
11	PC3/ADC13	PC12/U5_TX/SDIO_CK	53
12	VSSA	PC11/U4_RX/SDIO_D3	52
13	VDDA	PC10/U4_TX/SDIO_D2	51
14	PA0/WKUP/ADC0-TIM2_CH1_ETR/TIM5_CH1/TIM8_ETR	PA15/JTDI/SPI3_NSS/I2S3_WS	50
15	PA1/ADC1-TIM2_CH2-TIM5_CH2	PA14/JTCK/SWCLK	49
16	PA2/U2_TX/ADC2-TIM2_CH3-TIM5_CH3	VDD	48
17	PA3/U2_RX/ADC3-TIM2_CH4-TIM5_CH4		
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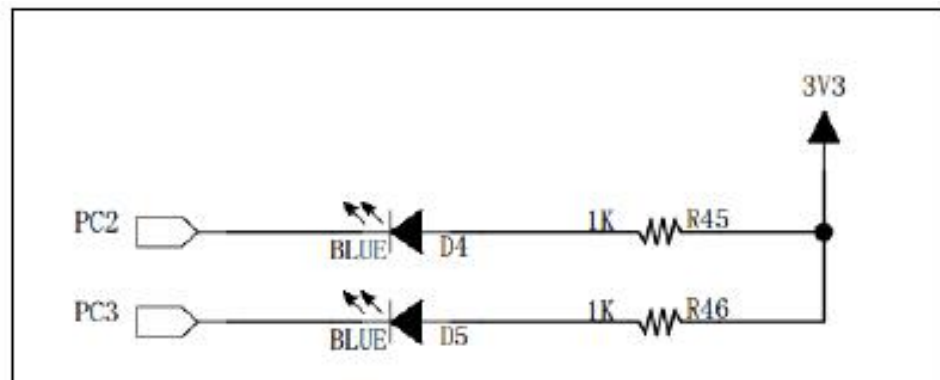
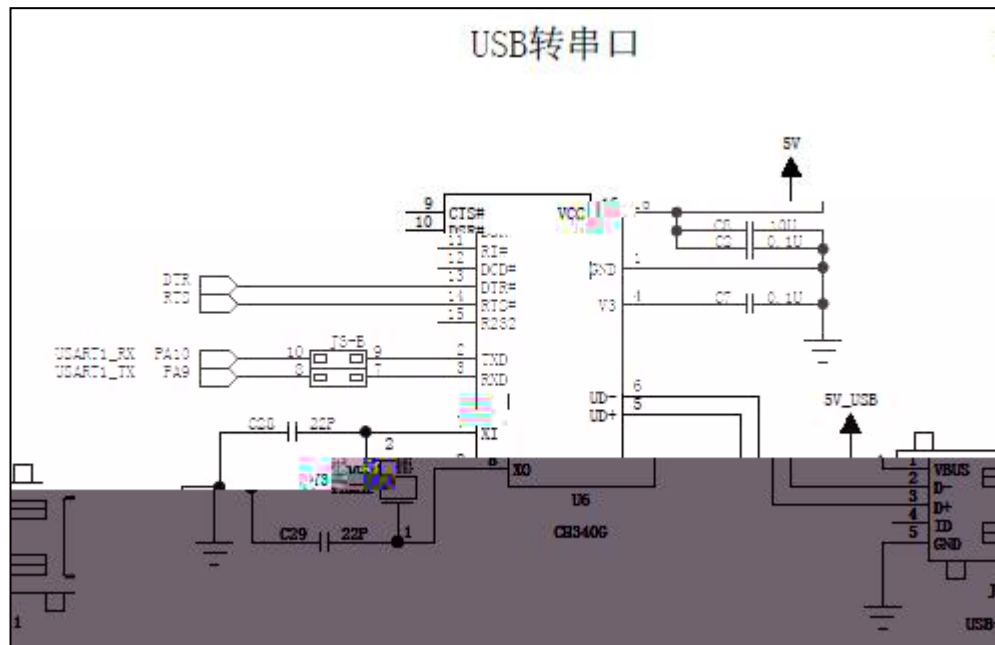


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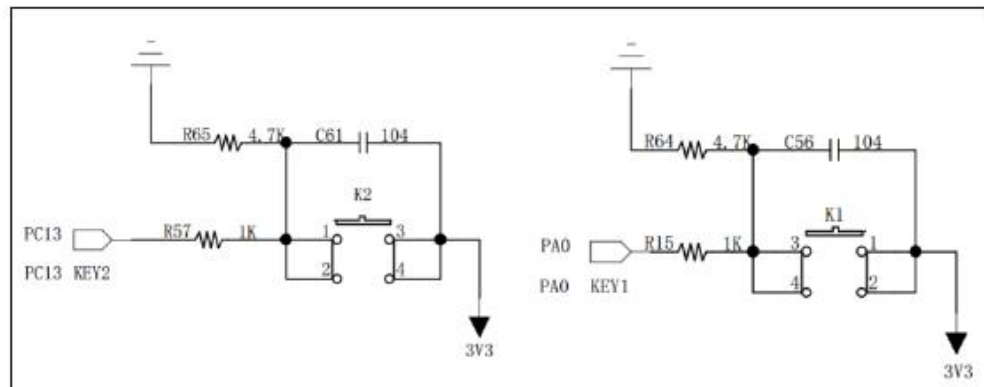
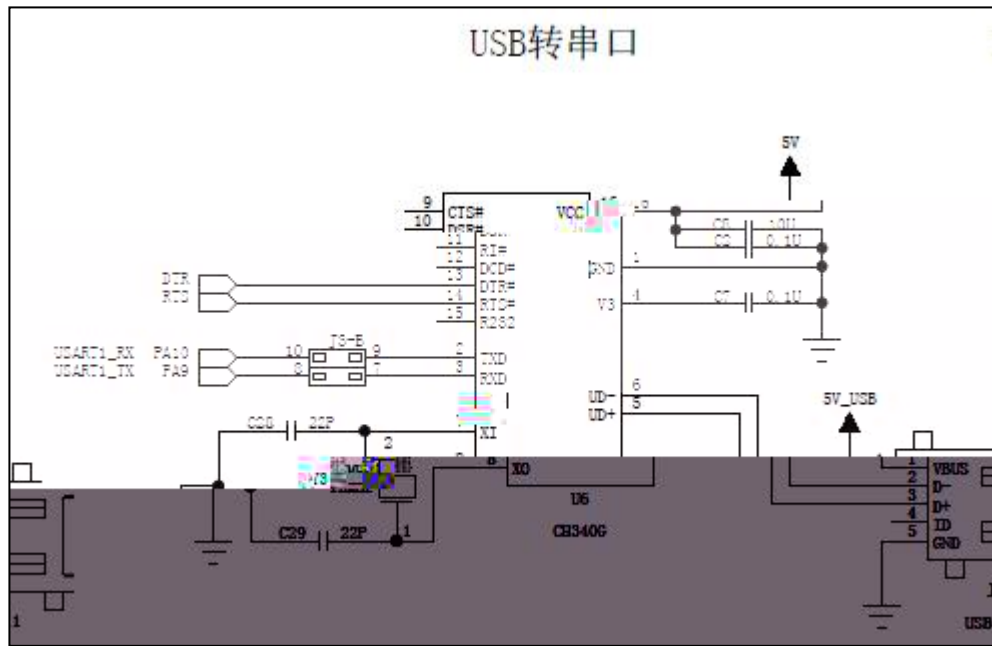
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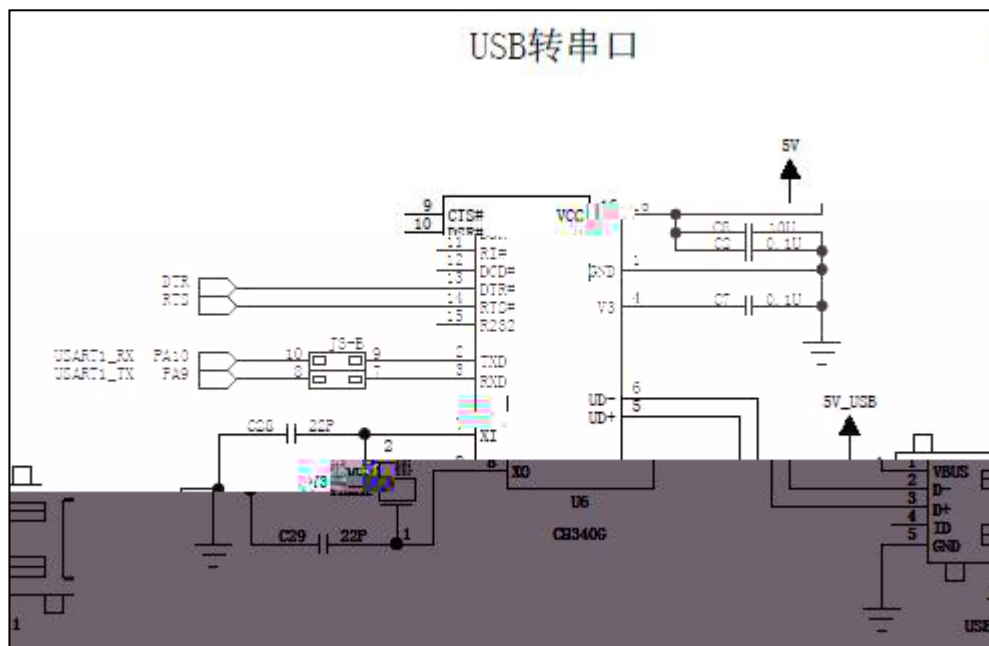


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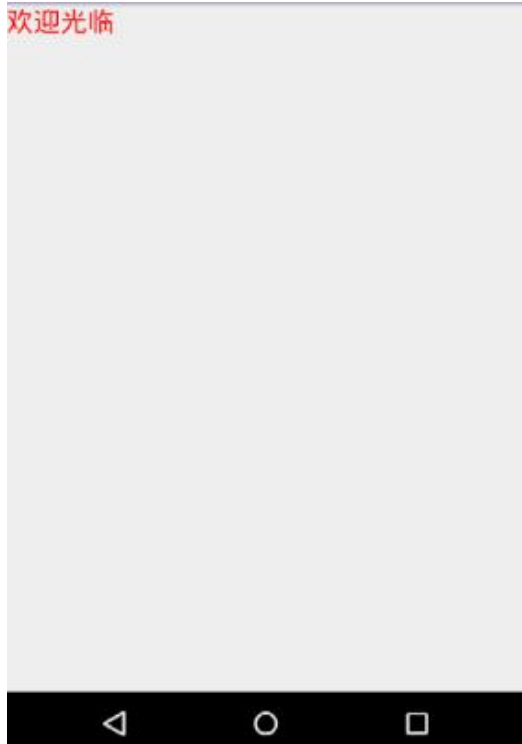
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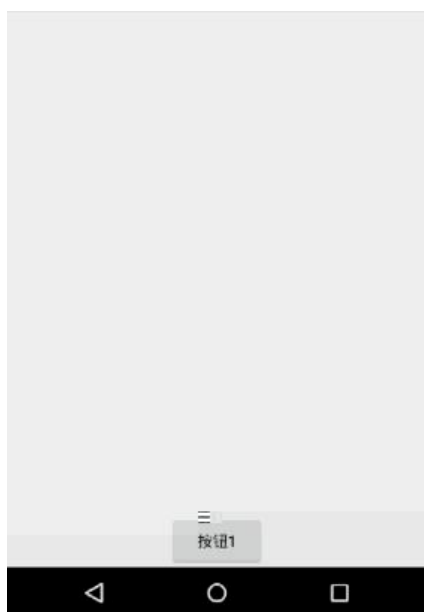
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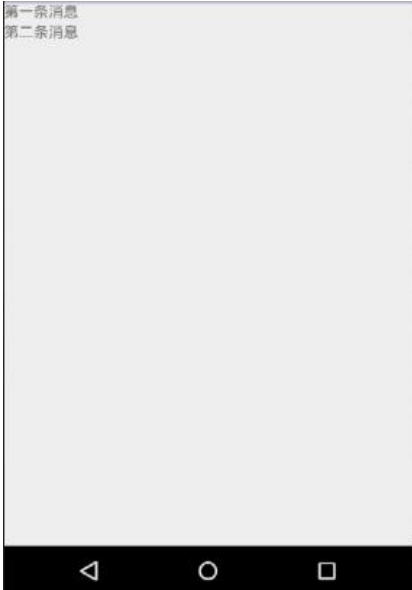
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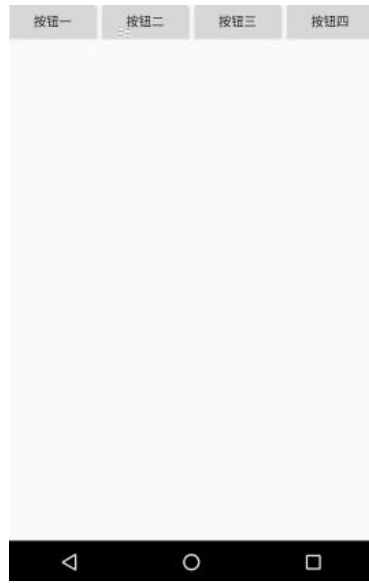
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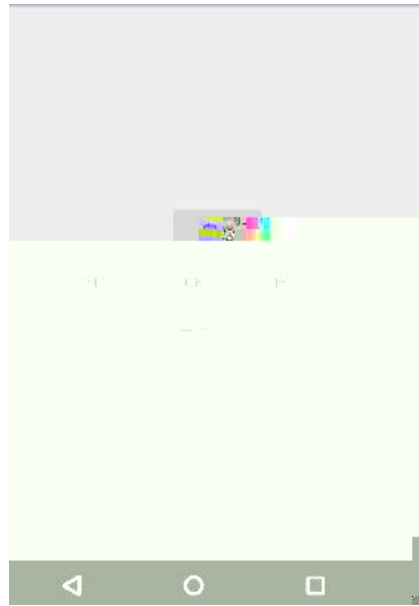


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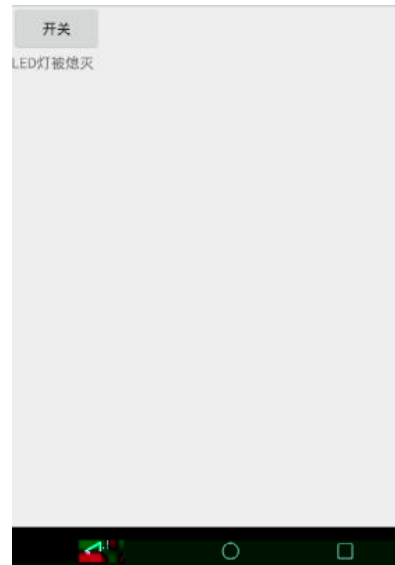
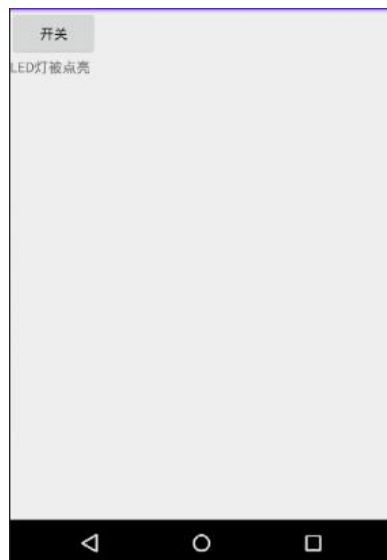
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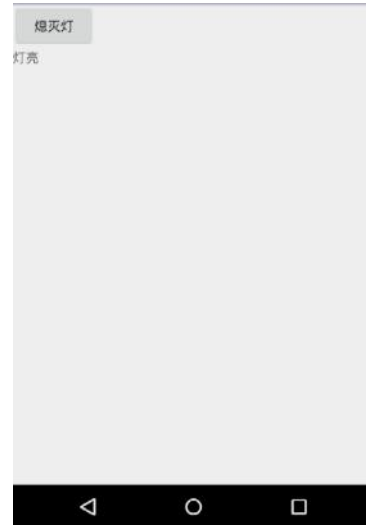
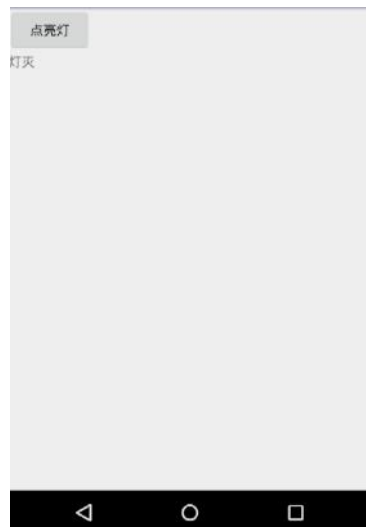
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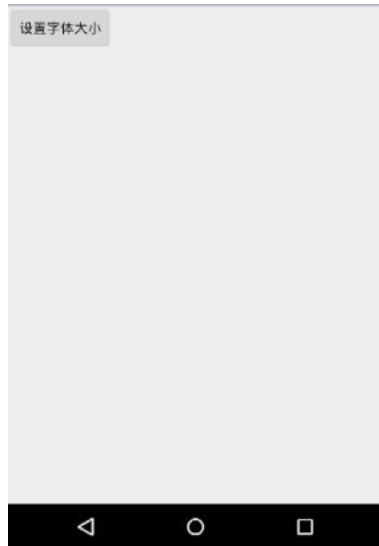
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